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Scuola Superiore Sant'Anna

Retis Real-Time Systems Laboratory

RETIS Seminars

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Via Moruzzi, 1 - Pisa

Cache Persistence Aware WCRT Analysis for Fixed Priority Preemptive Systems

Geoffrey Nelissen
Research Centre in Real-Time and Embedded Computing Systems (CISTER), Porto, Portugal

Abstract:

The introduction of caches in modern computing platforms is the cause of important variations in the execution time of each task, depending on whether the instruction and data it requires are already loaded in the cache or not. Many works have focused on analyzing the impact of preemptions on the worst-case execution time (WCET) and worst-case response time (WCRT) of tasks in preemptive systems. The preempted tasks may indeed suffer additional cache misses if its memory blocks are evicted from the cache during the execution of preempting tasks. These evictions cause extra accesses to the main memory, which result in additional delays in the task execution. This extra cost is usually referred to as cache-related preemption delays (CRPDs). Several approaches use information about the tasks' memory access patterns to bound and incorporate preemption costs into the WCRT analysis. These approaches still result in pessimistic WCRT bounds due to the fact that they do not consider the memory demand variation for successive instances of a same task. They usually assume that the useful cache content for the task is completely erased between two of its executions. However, in actual systems, successive instances of a task may re-use most of the data and instructions that were already loaded in the cache during previous executions.

This talk addresses the concept of persistent cache blocks from a task WCRT perspective, and will present how it can be used to reduce the pessimism of the WCRT analysis for fixed priority preemptive systems. Techniques exploiting this notion of cache persistence will be introduced to pre-configure systems to improve their runtime behavior.

Brief Bio

Geoffrey Nelissen earned his M.Sc. degree in Electrical Engineering at Université Libre de Bruxelles, Belgium, in 2008. He then worked during four years as a Ph.D. student in the PARTS research unit of ULB. In 2012, he received his Ph.D. degree under the supervision of Professors Joël Goossens and Dragomir Milojevic, on the topic "Efficient Optimal Multiprocessor Scheduling Algorithms for Real-Time Systems". He is currently workin g at CISTER, Porto, Portugal, as a research scientist in the area of real-time scheduling, embedded, distributed and safety critical system design and analysis.