

## DESIGNING MIXED CRITICALITY APPLICATIONS ON MODERN HETEROGENEOUS MPSOC PLATFORMS



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## **Abstract:**

Multiprocessor Systems-on-Chip (MPSoC) integrating hard processing cores with programmable logic (PL) are becoming increasingly more available. While these platforms have been originally designed for high performance computing applications, their rich feature set can be exploited to efficiently implement mixed criticality domains serving both critical hard real-time tasks, as well as soft real-time tasks. In this talk, we take a deep look at commercially available heterogeneous MPSoCs that incorporate PL and a multicore processor. We show how one can tailor these processors to support a mixed criticality system, where cores are strictly isolated to avoid contention on shared resources such as Last-Level Cache (LLC) and main memory. In order to avoid conflicts in last-level cache, we propose the use of cache coloring, implemented in the Jailhouse hypervisor. In addition, we employ ScratchPad Memory (SPM) inside the PL to support a multi-phase execution model for real-time tasks that avoids conflicts in shared memory. We provide a full-stack, working implementation on a latest-generation MPSoC platform, and show results based on both a set of data intensive tasks, as well as a case study based on an image processing benchmark application.

## **Short bio:**

Marco Caccamo is professor of Cyber-Physical Systems in Production Engineering at Technical University of Munich since 2018. He graduated in computer engineering at University of Pisa in 1997. He earned a PhD in computer engineering from Scuola Superiore Sant'Anna in 2002. Then, he joined University of Illinois at Urbana-Champaign, where he became full professor in 2014. He has chaired Real-Time Systems Symposium and Real-Time and Embedded Technology and Applications Symposium, the two IEEE flagship conferences on Real-Time Systems. His research activities focus on the areas of cyber-physical systems and real-time systems. He developed innovative software architectures and toolkits for the design automation of safe embedded digital controllers, and low-level resource management solutions for multicore architectures.

